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Radar Waveform Generator based on DDS

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Abstract- A radar waveform generator is implemented and it is designed by using directly digital modulation method based on DDS. It is able to generate arbitrary signals whose frequency amplitude and phases are controlled by the description words which will be given from external computer. Accurate waveforms are generated. By using Direct digital synthesis technique we can generate waveforms digitally . DDS technique is widely applicable and simple. Direct Digital Synthesizer (DDS) is a frequency synthesizer and it can generate arbitrary waveforms by using single, fixed-frequency reference clock. Some of the DDS Applications are: function generators, modulators. For implementing radar waveform generator along with DDS we need FPGA and PIC microcontroller. To generate the waveform using DDS we need to store the hexadecimal data into the internal registers of DDS chip along with that we need some control signals which will be generated using FPGA . First in PC we need to enter the information of the signal to be generated for that we need design a Graphical User Interface (GUI).In GUI we will enter the amplitude, frequency and phase of the waveform to be generated and then it has to covert that particular data into hexadecimal data based on the formulas mentioned in AD9910 datasheet, then it has to send that data to microcontroller through serial port. Now, microcontroller will receive that data from PC and then it has to send that data to the FPGA. FPGA will receive that data, along with that it has to generate some control signals and clock signals based on the control signals, received data has to be send to the internal registers of DDS chip.

Keywords: Direct Digital Synthesizer(DDS) ,Field Programmable Gate Array(FPGA),Graphical User Interface(GUI), microcontroller

I. INTRODUCTION

Generally for any equipment, it is important to readily produce and control accurate waveforms of different frequencies. Some of the examples include agile frequency sources with low spurious signal content and less phase noise for communications, which will be used for industrial and biomedical applications. For those applications, we should be capable of generating an adjustable waveform cost effectively and conveniently which is a key design consideration.

Several approaches are available for generating the signal but among those direct digital synthesis (DDS) is most flexible one. AD9910 DDS chip is used to generate an analog signal —usually a sine wave, but it can be used to generate other signals also by generating a time varying signal in digital form and then by using D/A converter we can generate an analog signal. As DDS devices offer faster switching between output frequencies and fine resolution in frequencies it is widely used.

As the technology advances in design and technology ,DDS devices consume less power and very compact .Here in this design we are using AD9910 DDS chip it can generate arbitary signals with frequencies ranging from 1Hz to 400 MHz (based on a 1-GHz clock), with time resolution of 64 bits. Devices with low cost and using new technologies are combined with DDS's which are used to generate waveforms and can be program them digitally—make DDS as attractive approach compared to other solutions. Multichannel RADAR waveform generator can be designed using multiple AD9910 DDS chips ,microcontroller and FPGA to control those AD9910 DDS chips. Here we are designing four channel waveform generator using 4 AD9910 DDS chips, which are used to produce four identical waveforms whose amplitude, phase and frequency can be varied digitally.

Here our main objective is to design a radar waveform generator. For this first we have to design a GUI where we have to enter the information required to generate an analog signal such as phase, frequency and amplitude and that information has to be converted into hexadecimal data based on the formulas mentioned in AD9910 datasheet and then it will be sent to the PIC microcontroller from PC using RS232 cable. By using that GUI we can also control the DDS chip. Microcontroller has to receive that hexadecimal data from the PC using serial port and then it has to send the data to FPGA through SPI. FPGA is used to generate some clock and control signals to DDS chips based on those control signals FPGA has to transfer that received hexadecimal data into the internal registers of DDS chips through SPI. Now that DDS will generate the signal based on that hexadecimal data stored in the internal registers.

II DDS TECHNOLOGY

Direct digital synthesis (DDS) is a technique for generating an arbitary waveforms such as sine wave by

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using time varying signal in digital form and then by using digital to analog converter we will generate an analog signal.DDS has ability to generate and control an accurate signal that's why it is used by the most of the industries. DDS technique is widely used for solving signal generation requirements for both communications and industrial based applications because we can generate an accurate analog signal using single chip with low cost and power consumption.

Fig1 shows the internal circuitry of a DDS device. its main components are phase-to-amplitude conversion (often a sine look-up table), phase accumulator and a DAC.

DDS can produces a sine wave at a given frequency. The frequency of the sinewave depends on two variables, the reference-clock frequency of the DDS and the binary number programmed into the internal registers (tuning word) of DDS.

Main input to the phase accumulator is frequency tuning word(FTW) i.e, binary number stored in the frequency register. If a sine look-up table is used, the phase accumulator will compute the phase(angle) address for look-up table,which will give the digital value of amplitude which corresponds to the sine of that phase angle to the DAC.Now, DAC will convert that digital value into corresponding value of analog voltage. To generate a sinewave of fixed frequency a constant value(it is determined by the binary number) is to be added to the phase accumulator for each clock cycle. If that constant value is large phase accumulator will step through the sine look-up table quickly and thus generate a high frequency sine wave.If that phase increment is small then phase accumulator will take more steps, accordingly it will generate a slower waveform.

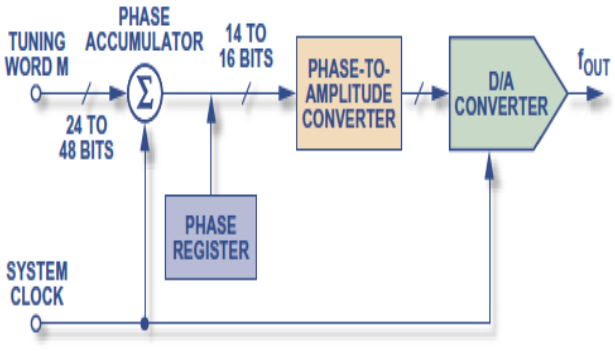

Fig1.Components Direct Digital Synthesizer

Operation principle of DDS can be easily understood with the Fig.1. Frequency tuning word is given as input to the Phase accumulator and converts it into angular phase and then it is converted into the sine wave amplitudes by using Amplitude/Sine Conv. Algorithm and then by using D/A converter analog sine wave is generated.

Here phase -to - amplitude lookup table will be used to convert the phase-accumulator's instantaneous output value (32 bits for AD9910)—Among those 32 bits unneeded less-significant bits will be eliminated by truncation—into the sine-wave amplitude information that will be applied to the (14 -bit) Digital to Analog converter. The architecture of DDS exploits the symmetrical nature of a sine wave as it utilizes mapping logic to synthesize a complete sine wave from one-quarter-cycle of data from the phase accumulator. The phase-to- amplitude lookup table will generate the remaining data by reading forward then backward through the lookup table. This is shown pictorially in Fig. 3.

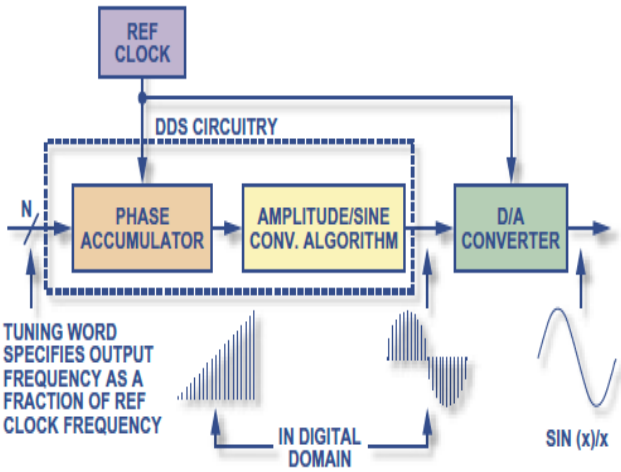

Fig2.Signal flow through DDS

To understand the basic function consider sine wave oscillations as a vector rotating around a phase wheel as shown in Fig.3. The number of discrete points on the wheel can be determined by the resolution of phase accumulator. Each discrete point on the phase wheel represents its corresponding equivalent point on cycle of sine wave.

As vector rotates around the wheel, corresponding output sine wave will be generated. One complete cycle of sinewave will be generated when vector completes one revolution at a constant speed around the phase wheel. The phase accumulator is used to provide the equivalent of the vector's linear rotation around the phase wheel.

Each content of the phase accumulator represents its corresponding point on the cycle of output sine wave. The number of phase points on the wheel will be determined by the resolution (N) of phase accumulator. The output of phase accumulator is linear so,we cannot directly generate any wave expect ramp. So, we will use phase-to-amplitude lookup table to convert output value of phase accumulator to sine wave amplitude information and then it will be

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applied to D/A converter. The output frequency and length of the accumulator are related by the equation.

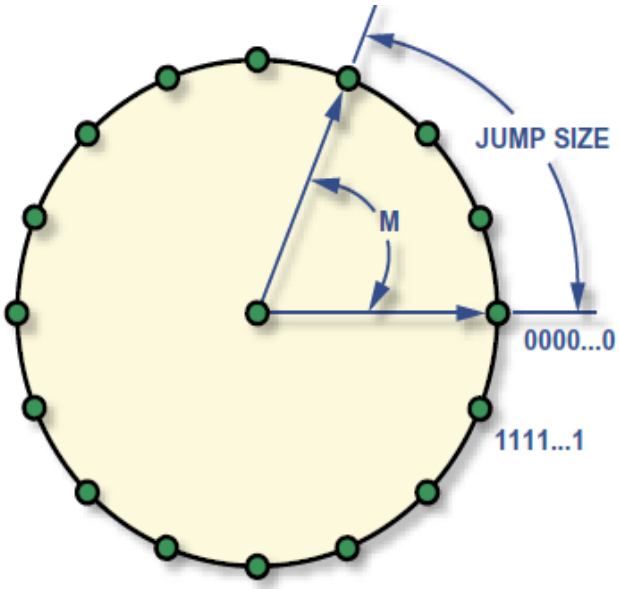
$$fo = \frac{M\ X\ fc}{2^N}$$

Where N denotes the number of bits used to represent the tuningword. Generally for AD9910 Frequency Tuning Word (FTW) is of 32 bit.
Where:

fo = output frequency of DDS

M = frequency tuning word

fc = internal clock frequency
N = length of the phase accumulator in bits



n	NUMBER OF POINTS
8	256
12	4096
16	65535
20	1048576
24	16777216
28	268435456
32	4294967296
48	281474976710656

Fig.3. Digital Phase Wheel

Here we are using AD9910 DDS chip it can generate waveforms whose frequencies are ranging from 1Hz to 400 MHz and clock frequency for AD9910 is 1 GHz and it has 14 bit Digital to Analog converter(DAC).

III SYSTEM ARCHITECTURE

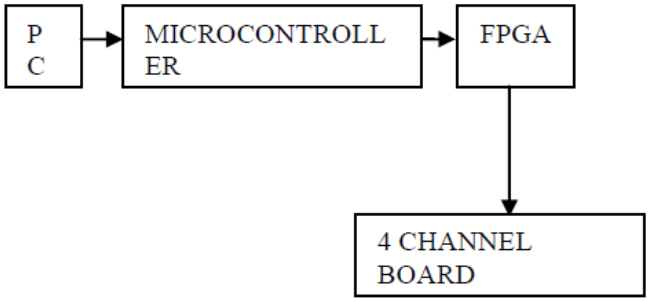


Fig.3. Block diagram

A *Graphical User Interface (GUI)*

By using DDS we are generating analog signals. In order to generate the analog signals using DDS we need to store the corresponding information(hexadecimal data) of the analog signal into the internal registers of DDS. so we need design GUI which acts like an interface between PC and microcontroller and it has to convert the corresponding information i.e, amplitude, frequency and phase into corresponding hexadecimal data using the formulas mentioned in the AD9910 datasheet.along with that GUI has to send that hexadecimal data to the microcontroller through serial port from the pc.

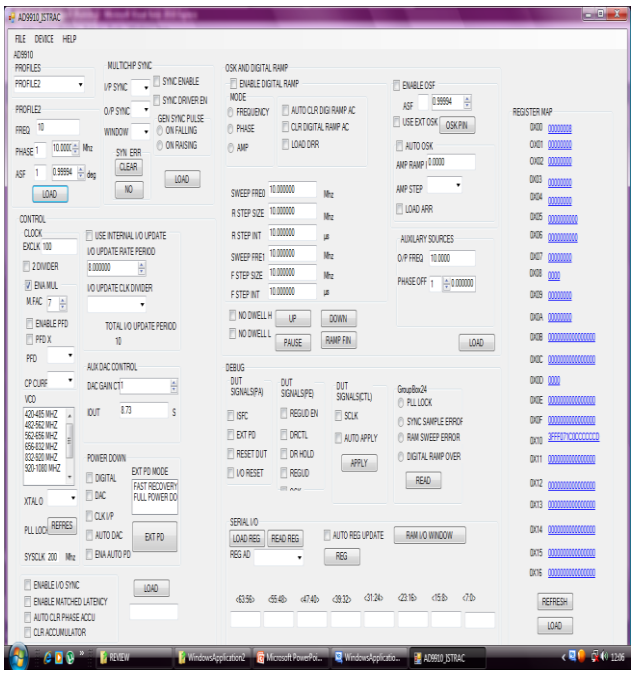


Fig.4. GUI

B *Microcontrller*

Here purpose of microcontroller is to receive the data sent from PC using GUI through serialport.we have to program the microcontroller such that it has to receive the data send

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by the pc through RS232 cable and then it has to send that hexadecimal data to the FPGA through serial peripheral interface(SPI). Here we are using DSPIC33F microcontroller.By using UART functions of DSPIC33F we can receive and store the data available at the serial port and by using SPI we can send that data to the FPGA.Here we are programming the DSPIC33F using MPLAB IDE and then by using PIC KIT3 programer,code will be dumped into the microcontroller.Fig.5. shows the compilation of the program written for the DSPIC33F in C language.

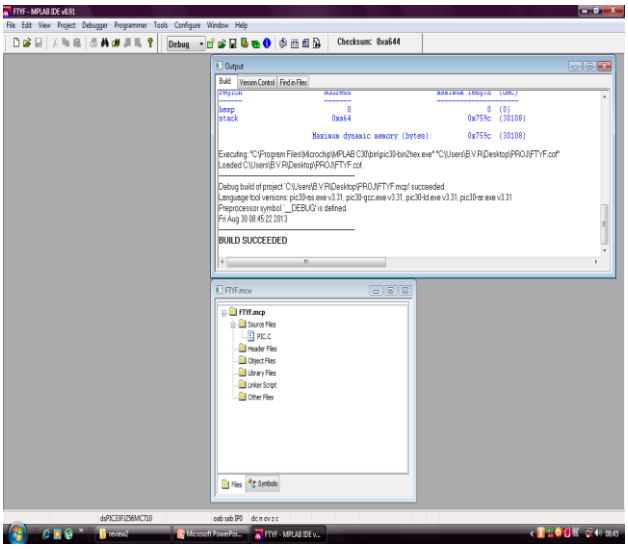

Fig.5. Compilation Of The C Program

C *Field Programmable Gate Array (FPGA)*

Here purpose of FPGA is to receive the data send from microcontroller through serial peripheral interface(SPI) and then it has to send that hexadecimal data into internal registers of AD9910 DDS chips through SPI based on some control signals,along with that it has to generate some clock signals to the AD9910 DDS chips.. PIC will send the hexadecimal data received from the PC to the FPGA through SPI.

We have to program the FPGA such that it has to receive that hexadecimal data sent from microcontroller and then based on some control signals such as IO_UPDATE it will send the data to DDS through SPI.FPGA is also used to generate clock signals using Digital Clock Manager(DCM).It will generate 10 mhz clock using its internal oscillator.Fig.6. shows the simulation of the code written in VHDL.

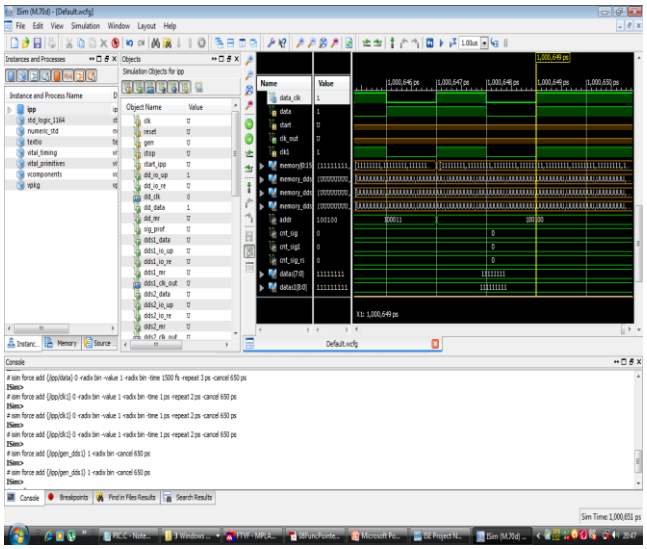

Fig.6. Simulation Of FPGA Code

D *Four Channel Board*

Here in this project our goal is to generate identical signals whose amplitude, phase and frequency should be varied according to our requirement. so for generating identical signals we need to synchronize DDS chips.

DDS chips has to generate the signals at a time i.e, they should start generating the analog signals at the same time so, that the analog signals will be synchronized. For synchronizing the DDS chips one of the DDS has to generate SYNC_CLK and ADCLK846 will distribute that SYNC_CLK to all the AD9910 DDS chips.

One which Generate the SYNC_CLK acts like master and the remaining DDS chips will behave as slaves, thus the internal blocks of DDS chips are synchronized to single clock frequency i.e, they will operate on the same internal clock so they will produce identical signals. SYNC_CLK will be generated from the internal clock of the master only by using frequency divider. AD9520 will be used to distribute the clock signal generated by the FPGA to all the DDS chips. FPGA will provide the 10 MHz signal, but AD9910 need 1 Ghz clock frequency so, we will multiply the 10Mhz signal using PLL multiplier to get desired 1 Ghz frequency.

By using these devices the multichannel RADAR waveform generator is implemented. Now in the GUI we have to specify the amplitude, phase and frequency of the desired signal and we need set the mode of the AD9910 DDS chip in which it has to operate generally DDS chip will operate in single tone mode in which DDS is used to generate the signal based on the information present in its internal registers . After setting all the controls of DDS chips in GUI,it will generate corresponding hexadecimal data and then it will be send to the microcontroller.Now microcontroller will receive that data through serialport and then it will send that data to FPGA through SPI and then FPGA will receive that data and send it to the the internal registers of DDS.

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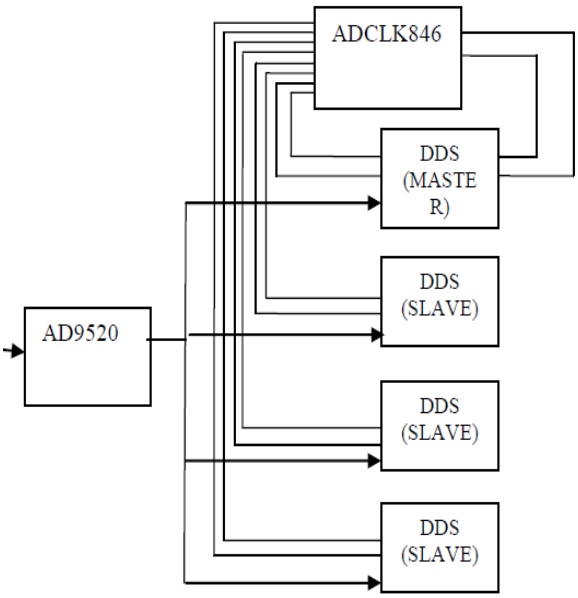

Fig.7. 4 channel board

IV RESULTS

The below figure shows output of DDS applied to AGILENT spectrum analyzer. It shows single frequency output spectrum in which mark1 specifies the frequency of signal which is 35 Mhz with an amplitude of 14.210 dbm.

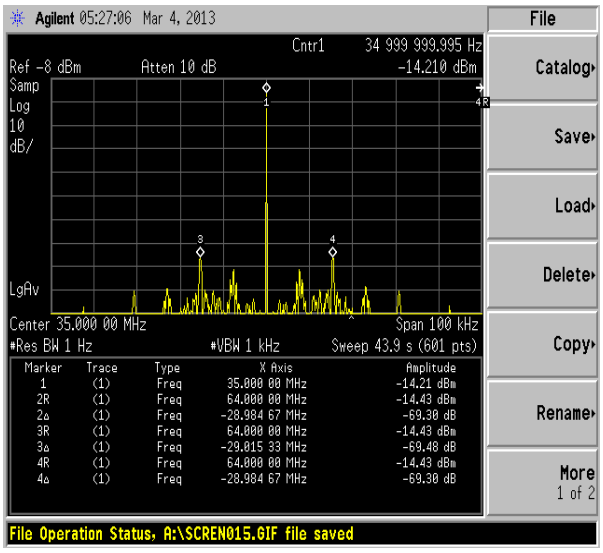

Fig.8. Single frequency output spectrum

Below figure shows AD9910 DDS output which is directed into spectrum analyzer and zoomed in.

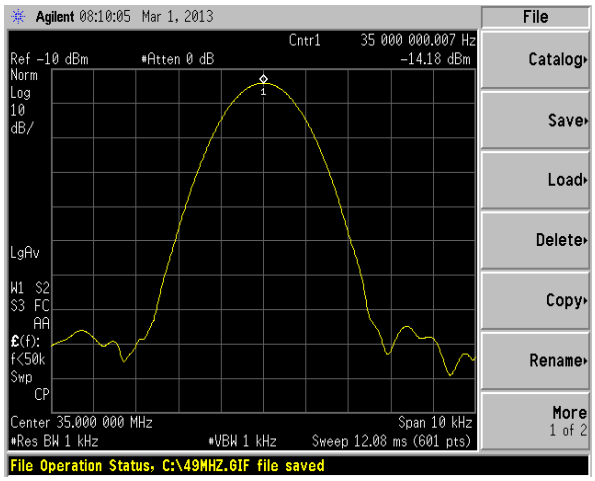

Fig.9. DDS output direct into spectrum analyzer

Below Fig.10. shows the sinewave output generated by AD9910 DDS whose output frequency is 50MHz.

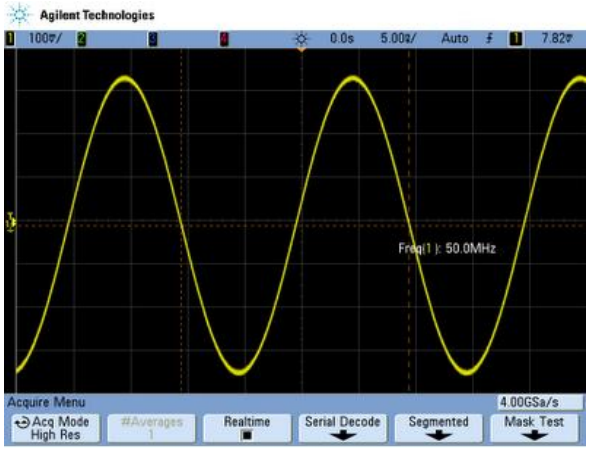

Fig.10. Sinewave output of DDS

Below Fig.11. shows the sinewave outputs generated by two different DDS chips.

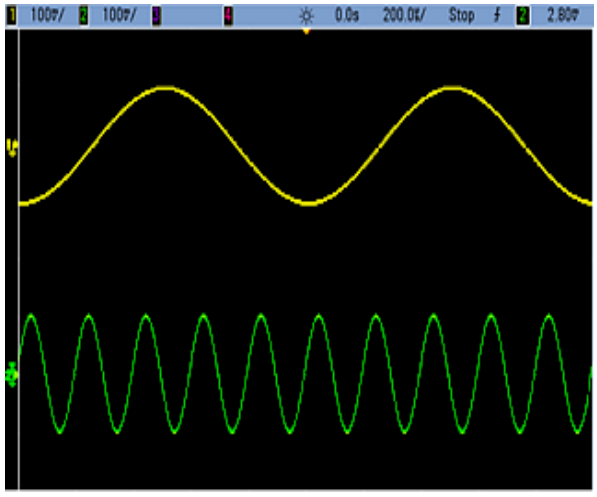

Fig.8. Sinwave outputs of two different DDS chips

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V CONCLUSION

In this paper, the Four channel waveform generator is designed using Four AD9910 DDS chips. This design shows the architecture of multichannel radar waveform generator which is designed using AD9910 DDS chips, FPGA and PIC microcontroller.

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BIOGRAPHY

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